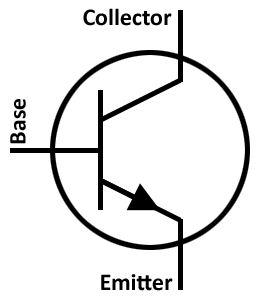
Transistors:

In a transistor, a small base current can switch on a GREATER current through the collector.

To work out the current coming out of the emitter:

**Ie = Ib + Ic**



Logic Gates:

|  |  |  |
| --- | --- | --- |
| **Type of Gate** | **Symbol** | **Explanation** |
| AND | 8fa676e743afd1730affa37aa0de2dc587021906.gif | To give a high output, both A **and** B must have a high output or be on. AND gates are like two switches in series; the circuit can’t work if one switch is off. |
| OR | d54b529f27568c81cca1caff755793f853e9cd4e.gif | To give a high output, one of A **or** B must have a high output or be on. OR gates are like two switches in parallel; only one switch needs to be on for the circuit to work. |
| NOT | f0a2797c09c4ca7f456edf2c2b27d587c9f5abab.gif | To give a high output, the input must be low or completely off. NOT gates will give the opposite of the (single) input – the output is **not** what the input is. |

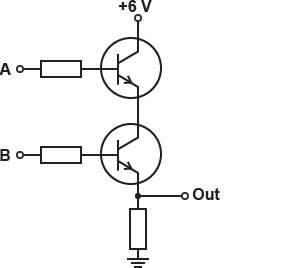
Making an AND gate:

Two transistors can be combined to make an AND gate.

1. A small input at A will switch on the upper transistor.
2. A small input at B will switch on the lower transistor.
3. A current at A **and** at B are needed to switch on the 6V supply.

The other logic gates can be made by using different combinations of transistors.

Transistor circuits ALWAYS have a high value resistor in the base circuit to limit the current.



NAND and NOR gates:

|  |  |  |
| --- | --- | --- |
| **Type of Gate** | **Symbol** | **Explanation** |
| NAND | 2_18_1_4.png | It behaves like an AND gate followed by a NOT gate. |
| NOR | 2_18_2_4.png | It behaves like an OR gate followed by a NOT gate. |

Truth Tables:

Truth tables show how logic gates behave.

* When there is some input (or output), a 1 is entered in the table
* When there is NO input (or output), a 0 is entered in the table

AND Gate: OR Gate:

|  |  |  |
| --- | --- | --- |
| **Input A** | **Input B** | **Output** |
| 0 | 0 | 0 |
| 1 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 1 | 1 |

|  |  |  |
| --- | --- | --- |
| **Input A** | **Input B** | **Output** |
| 0 | 0 | 0 |
| 1 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 1 | 1 |

NAND Gate: NOR Gate:

|  |  |  |
| --- | --- | --- |
| **Input A** | **Input B** | **Output** |
| 0 | 0 | 1 |
| 1 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 1 | 0 |

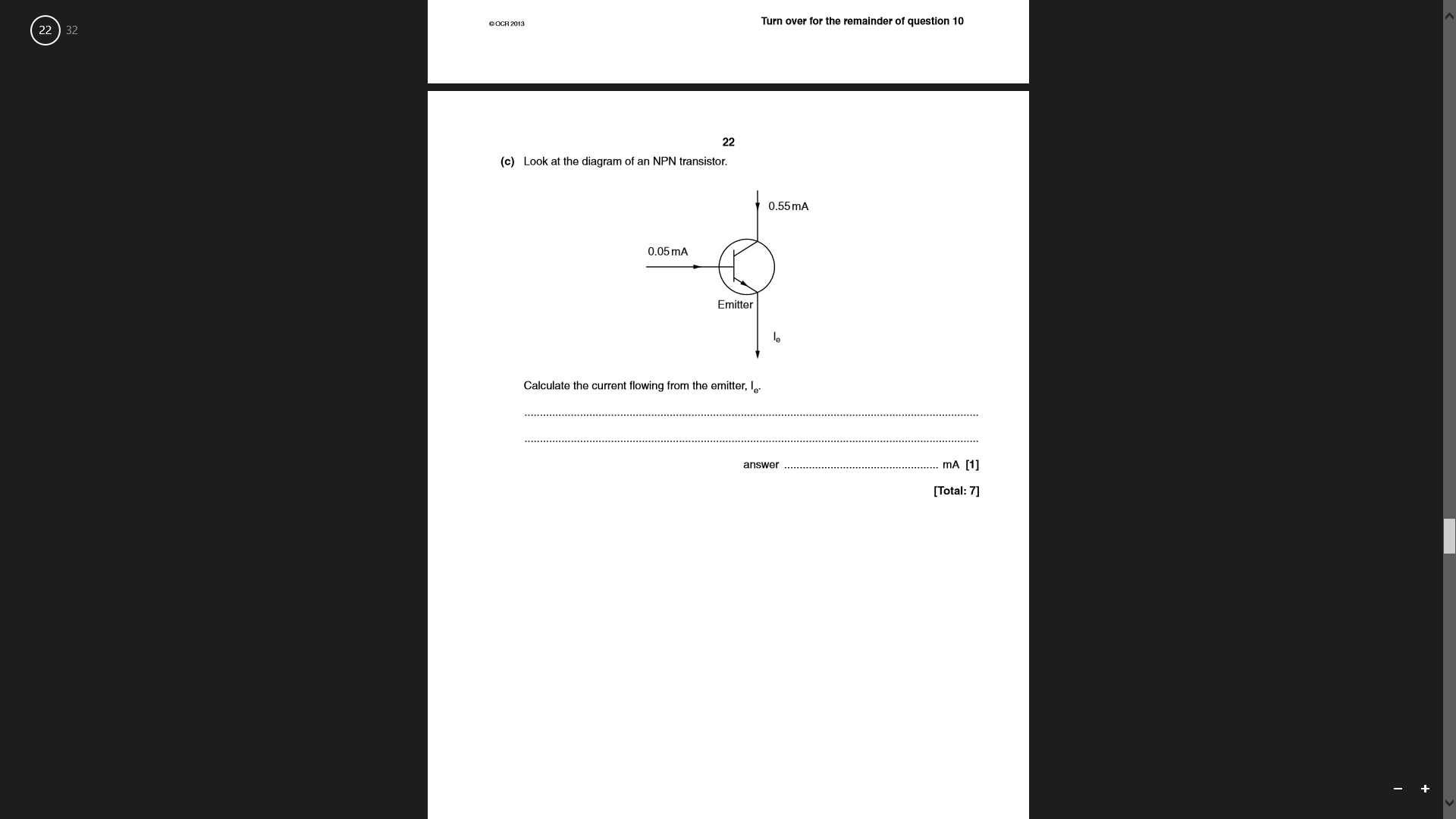
|  |  |  |
| --- | --- | --- |
| **Input A** | **Input B** | **Output** |
| 0 | 0 | 1 |
| 1 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 1 | 0 |

NOT Gate:

|  |  |
| --- | --- |
| **Input A** | **Output** |
| 0 | 1 |
| 1 | 0 |

Past Papers:

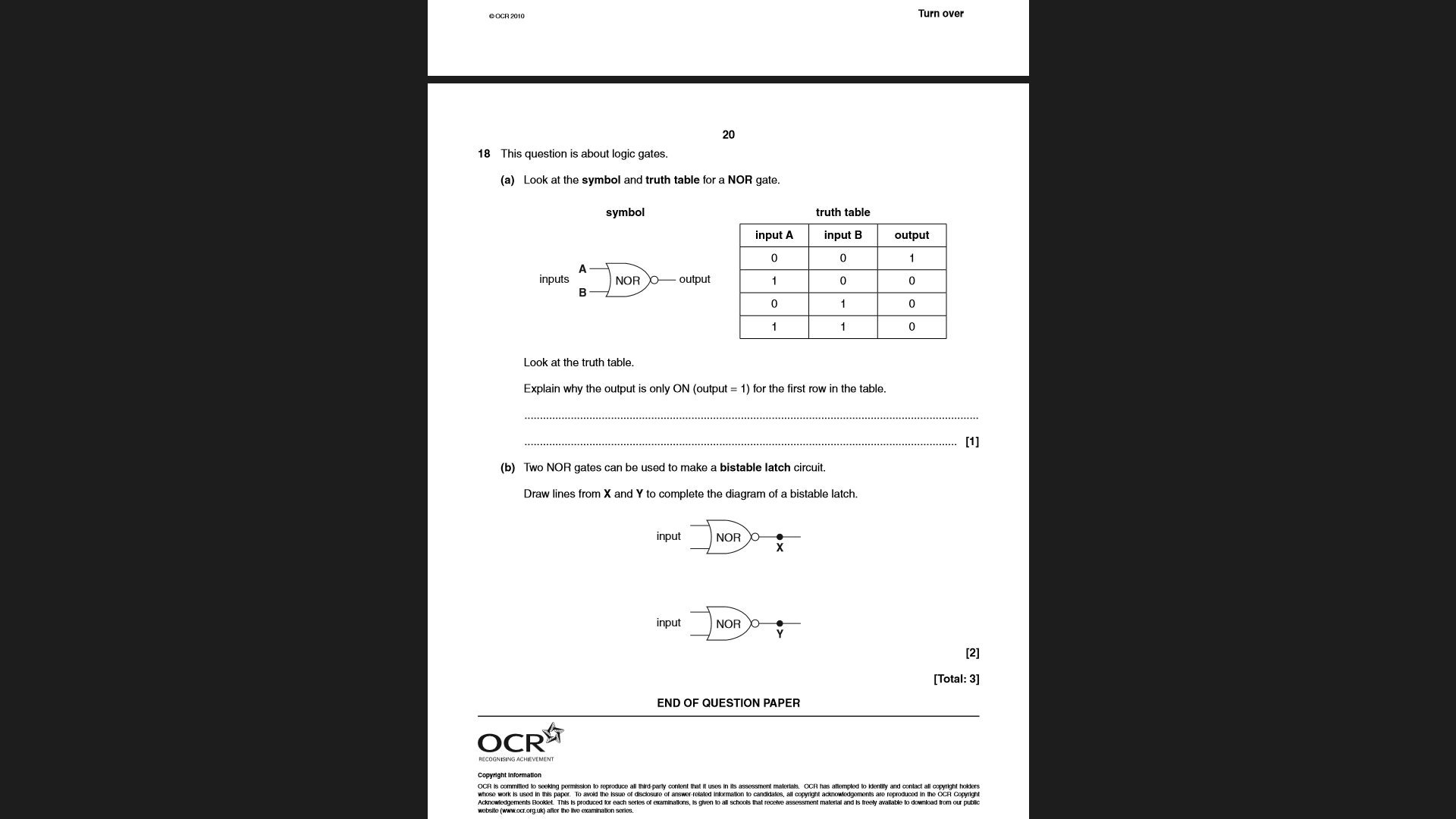
PPQ(1):



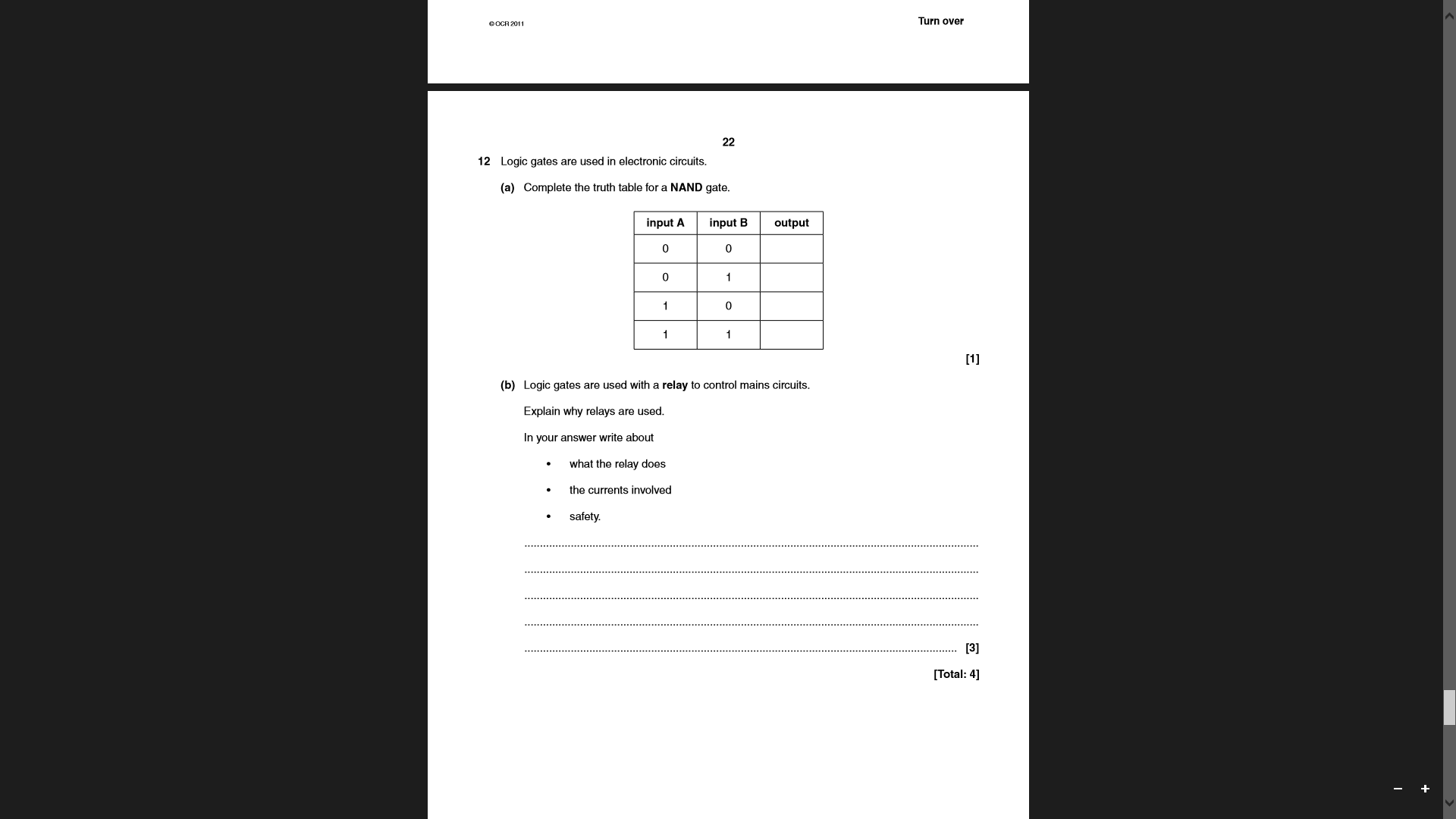
PPQ(2):



PPQ(3):

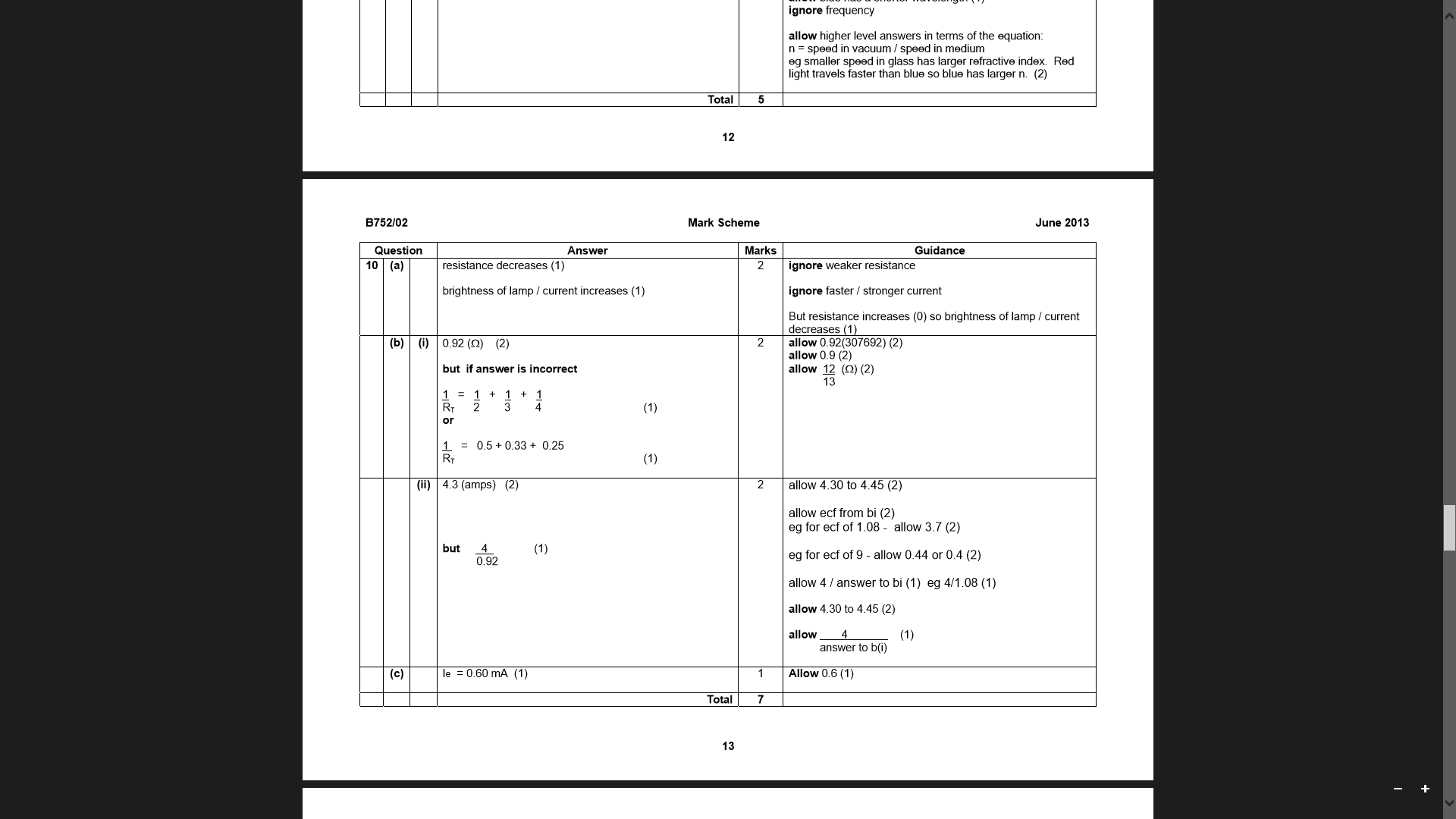


PPQ(4):

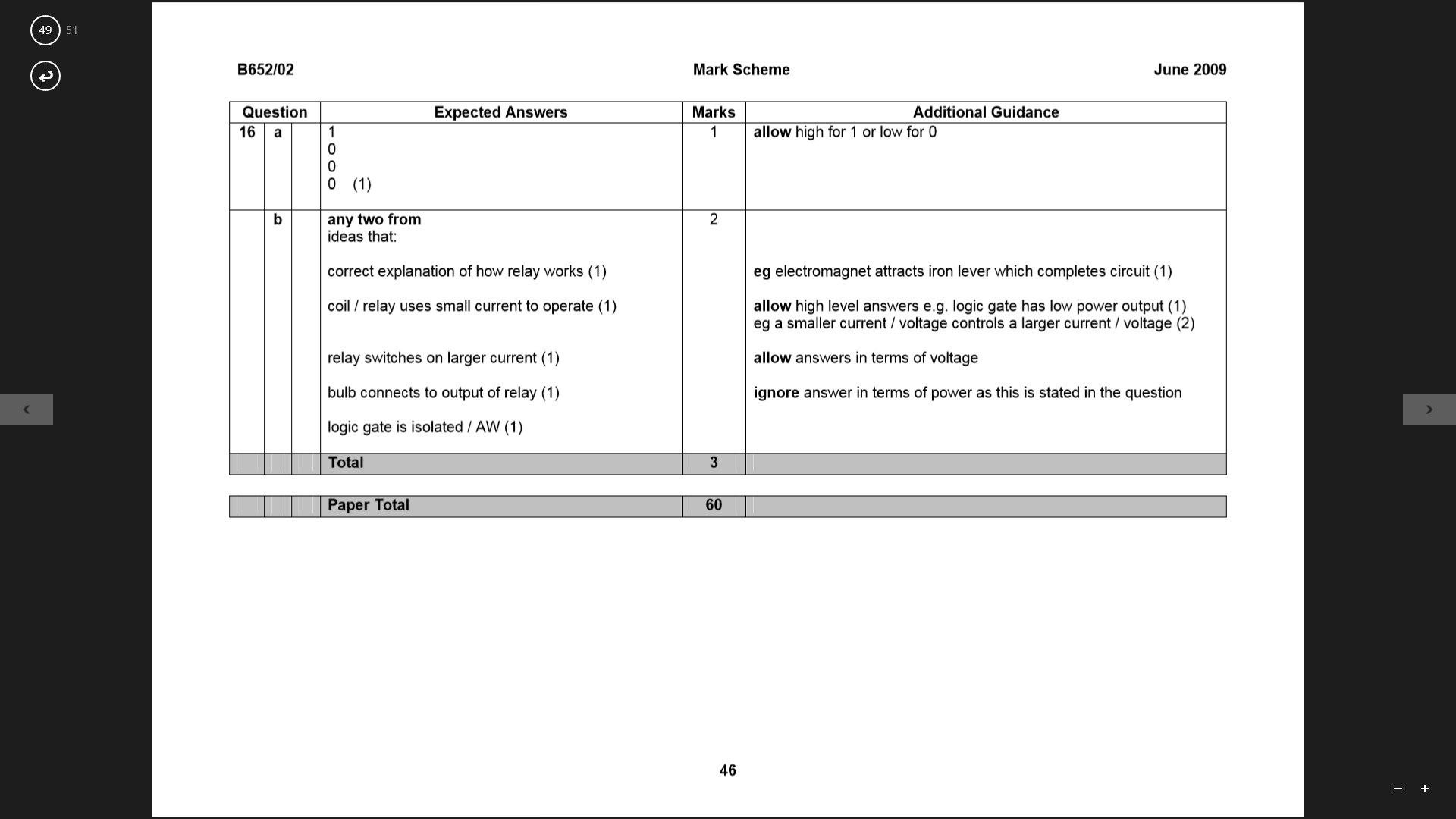


Mark Schemes:

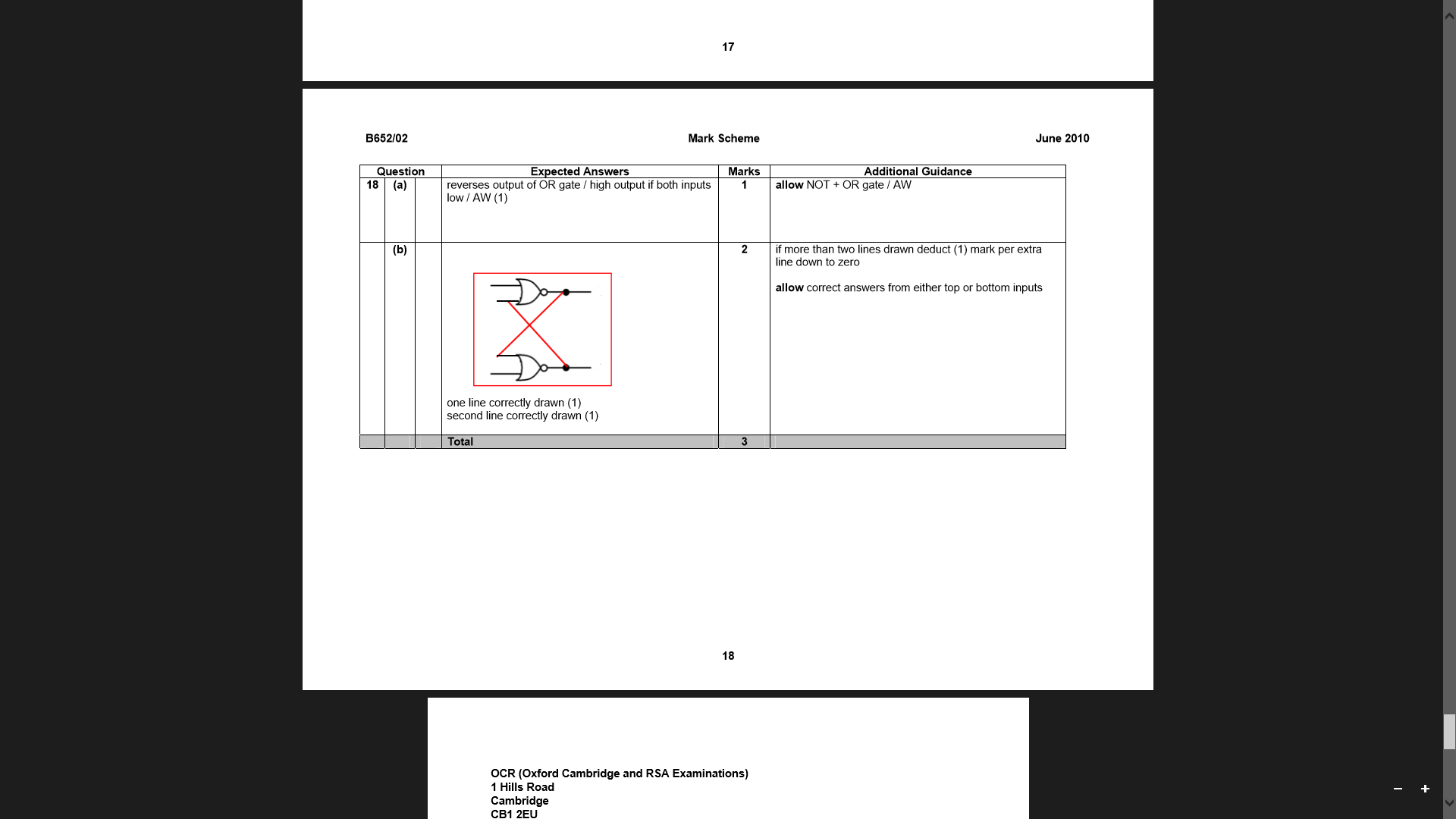
PPQ(1):



PPQ(2):



PPQ(3):



PPQ(4):

